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AMENDMENTS TO THE CLAIMS:

Please cancel claims 32, 36, 39 and 54 without prejudice or disclaimer.

- 1. (Currently amended) A semiconductor device, comprising:
- a multi-layered insulation film formed on a semiconductor substrate, said multi-layered insulation film comprising:
- a first insulation layer comprising an organosiloxane film having a dielectric constant which is lower than a silicon oxide dielectric constant;
- a second insulation layer comprising a polysiloxane compound having an Si-H group and formed on and adhering to a top of said organosiloxane film of said first insulation layer; and
- a third insulation layer comprising an inorganic material and formed on and adhering to a top of said second insulation layer; and
- a plurality of wires which are formed in grooves formed in said multi-layered insulation film, said multi-layered insulation film filling a space between said wires,
- wherein said <u>organosiloxane film comprises a methyl silsesquioxane (MSQ) laver, and said polysiloxane compound second insulation layer comprises a methylated hydrogen silsesquioxane (MHSQ) layer which adheres to said <u>MSQ layer organosiloxane film</u> and said inorganic material.</u>
- 2. (Canceled)
- 3. (Canceled)
- 4. (Previously Presented) The semiconductor device according to claim 1, wherein said third insulation layer comprises at least one material selected from the group consisting of silicon oxide, silicon nitride and silicon oxymitride.
- 5. (Currently amended) A semiconductor wafer, comprising:

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a multi-layered insulation film formed on a surface of the wafer, said multi-layered insulation film comprising:

a first insulation layer comprising an organosiloxane film having a dielectric constant which is lower than a silicon oxide dielectric constant;

a second insulation layer comprising a polysiloxane compound having an Si-H group and formed on and adhering to a top of said organosiloxane film of said first insulation layer; and

a third insulation layer comprising an inorganic material and formed on and adhering to a top of said second insulation; and

a plurality of wires which are formed in grooves formed in said multi-layered insulation film, said multi-layered insulation film filling a space between said wires,

wherein said organosiloxane film comprises a methyl silsesquioxane (MSO) layer, and said polysiloxane compound second insulation layer comprises a methylated hydrogen silsesquioxane (MHSQ) layer which adheres to said MSQ layer organosiloxane film and said inorganic material.

- 6. (Canceled)
- 7. (Canceled)
- 8. (Previously Presented) The semiconductor wafer according to claim 5, wherein said third insulation layer comprises at least one material selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride.
- 9-30 (Canceled)
- 31. (Previously Presented) The semiconductor device according to claim 1, wherein said dielectric constant of said first insulation layer is no greater than 3.5.

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- 32. (Canceled)
- 33. (Canceled)
- 34. (Previously presented) The semiconductor device according to claim 1,

wherein said first insulation layer comprises a thickness greater than a thickness of said second insulation layer, and

wherein said first insulation layer comprises a thickness greater than a thickness of said third insulation layer.

35. (Currently amended) The semiconductor device according to claim 1, <u>further comprising:</u>

<u>another layer formed in wherein said second insulation layer comprises a first layer and a second layer placed in said first layer.</u>

- 36. (Canceled)
- 37. (Previously Presented) The semiconductor device according to claim 1, wherein a bottom of said groove is formed on a same surface as said first insulation layer.
- 38. (Previously Presented) The semiconductor device according to claim 1, wherein said plurality of wires comprise copper wires.
- 39. (Canceled)
- 40. (Currently amended) The semiconductor device according to claim 42, wherein said MHSQ layer film comprises a thickness of about 50 nm.
- 41. (Currently amended) A semiconductor device having a damascene wiring structure, said semiconductor device comprising:

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a multi-layered insulation film formed on a semiconductor substrate, said multi-layered insulation film having a plurality of recesses and comprising:

a first insulation layer comprising an organosiloxane film having a dielectric constant which is lower than a silicon oxide dielectric constant;

a second insulation layer comprising a polysiloxane compound having an Si-H group and formed on and adhering to a top of said organosiloxane film of said first insulation layer; and

a third insulation layer comprising an inorganic material and formed on and adhering to a top of said second insulation layer; and

an electroconductive film formed in a recess in said plurality of recesses, said multilayered insulation film filling a space between recesses in said plurality of recesses,

wherein said organosiloxane film comprises a methyl silsesquioxane (MSQ) layer, and said polysiloxane compound second insulation layer comprises a methylated hydrogen silsesquioxane (MHSQ) layer which adheres to said MSQ layer organosiloxane film and said inorganic material.

- 42. (Currently amended) A semiconductor device comprising a multi-layered insulation film and a plurality of wires formed on a semiconductor substrate, said multi-layered insulation film comprising:
- a first insulation layer comprising an organosiloxane film having a dielectric constant which is lower than a silicon dioxide dielectric constant;
- a second insulation, adhesive layer comprising a polysiloxane compound having an Si-H group and formed on and being in contact with a top of said organosiloxane film of said first insulation layer; and
- a third insulation layer comprising an inorganic material and formed on and being in contact with a top of said second insulation, adhesive layer,

wherein said multi-layered insulation film fills a space between said wires in said plurality of wires,

wherein said plurality of wires are formed in grooves which are formed in said multi-

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layered insulation film, and

wherein said <u>organosiloxane film comprises a methyl silsesquioxane (MSO) layer, and said polysiloxane compound</u> second insulation layer comprises a methylated hydrogen silsesquioxane (MHSQ) layer which adheres to said <u>MSQ layer organosiloxane film</u> and said inorganic material.

- 43. (Currently amended) The semiconductor device according to claim 1, wherein said first insulation layer, said second insulation layer and said third insulation layer of said multi-layered insulation film comprise substantially uniform widths.
- 44. (Previously presented) The semiconductor device according to claim 1, wherein a surface of said third insulation layer is substantially coplanar with a surface of said plurality of wires.
- 45. (Previously Presented) The semiconductor device according to claim 1, wherein said second insulation layer is formed by one of a plasma CVD and a spin coating process where said semiconductor substrate is continuously maintained in a plasma atmosphere.
- 46. (Currently amended) The semiconductor device according to claim 1, wherein said methylated hydrogen silsesquioxane (MHSQ) layer includes methylated hydrogen silsesquioxane (MHSQ) having repeating units shown by formulae I, II and III

$$\begin{bmatrix}
c_{H_3} \\
c_{-\frac{1}{2}i} \\
c_{-\frac{1}{2}i}
\end{bmatrix}$$

$$\begin{bmatrix}
d \\
c_{-\frac{1}{2}i} \\
c_{-\frac{1}{2}i}
\end{bmatrix}$$

$$\begin{bmatrix}
d \\
c_{-\frac{1}{2}i} \\
c_{-\frac{1}{2}i}
\end{bmatrix}$$

$$\begin{bmatrix}
c_{H_3} \\
c_{H_3}
\end{bmatrix}$$

$$\begin{bmatrix}
c_{H_3} \\$$

, and

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wherein a molar ratio of $[\Pi]$ to a total of I_{\bullet} [[.]] Π and Π is at least 0.2.

- 47. (Currently amended) The semiconductor device according to claim 1, wherein a greatest thickness of a thickest portion of said second insulation layer is less than a thickness of said first insulation layer.
- 48. (Currently amended) The semiconductor device according to claim 1, wherein said second insulation layer comprises a thin layer for adhering said third insulation layer to said first insulation layer.
- 49. (Currently amended) A semiconductor device, comprising:
- a multi-layered insulation film having a plurality of grooves formed therein, said multilayered insulation film comprising:
- a first insulation layer formed on a substrate and comprising an organosiloxane film having a dielectric constant which is lower than a silicon oxide dielectric constant;
- a second insulation layer comprising a methylated hydrogen silsesquioxane (MHSQ) layer having an Si-H group and formed on said organosiloxane film of said first insulation layer; and
- a third insulation layer comprising an inorganic material and formed on said second insulation layer; and
- a plurality of wires which are formed in grooves formed in said multi-layered insulation film, said multi-layered insulation film filling a space between said wires,
- wherein said organosiloxane film comprises a methyl silsesquioxane (MSQ) layer, and said methylated hydrogen silsesquioxane (MHSQ) layer adheres to said MSQ layer organosiloxano film and said inorganic material.
- (Currently amended) The semiconductor device according to claim 49, further 50. comprising:
 - a plurality of gate electrodes formed on said substrate, said first insulation layer being

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formed on and between said gate electrodes,

wherein said plurality of wires comprises a contact which contacts a diffusion region formed in said substrate between said plurality of gate electrodes, and

wherein a space formed between adjacent gate electrodes in said plurality of gate electrodes is filled with said first insulation layer.

- 51. (Previously presented) The semiconductor device according to claim 50, wherein a space formed between adjacent gate electrodes in said plurality of gate electrodes is filled with said first insulation layer.
- 52. (Previously presented) The semiconductor device according to claim 1, wherein said first, second and third insulation films of said multi-layered insulation film fill a space between said wires.
- 53. (Previously presented) The semiconductor device according to claim 1, further comprising:

a silicon nitride layer, said first insulation layer being formed on said silicon nitride layer and said plurality of grooves having a bottom defined by an upper surface of said silicon nitride layer.

- 54. (Canceled)
- 55. (Previously presented) The semiconductor device according to claim 1, wherein said first, second and third insulation layers fill an entire space between said grooves.
- 56. (Previously presented) The semiconductor device according to claim 1, further comprising:
 - a plurality of gate electrodes formed on said semiconductor substrate; and a plurality of impurity diffusion regions formed in the semiconductor substrate,

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wherein said first, second and third insulation layers are formed on said plurality of gate electrodes, and

wherein said plurality of grooves comprises a plurality of contact holes formed in said first, second and third insulation layers on said plurality of impurity diffusion regions and between said plurality of gate electrodes.